SBAC-PAD 2015
27th International Symposium on Computer Architecture and High Performance Computing

October 18-25
Florianópolis, Santa Catarina, Brazil

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SATELLITE EVENTS

10th Marathon of Parallel Programming

Calebe de Paula Bianchini (Mackenzie Presbyterian University, Brazil)

4th Workshop on Parallel Programming Models (MPP)

Leandro A. J. Marzulo (State University of Rio de Janeiro, Brazil)

Felipe França (Federal University of Rio de Janeiro, Brazil)

6th Workshop on Applications for Multi-Core Architectures (WAMCA)

Claude Tadonki (Mines-Paris, France)

Cristiana Bentes (State University of Rio de Janeiro, Brazil)

Guido Araujo (University of Campinas, Brazil)

Lucia Drummond (Federal Fluminense University, Brazil)

Mauricio Pilla (Federal University of Pelotas, Brazil)

Phillippe O. A. Navaux (Federal University of Rio Grande do Sul, Brazil)

Ricardo Farias (Federal University of Rio de Janeiro, Brazil)

X Workshop sobre Educação em Arquitetura de Computadores (WEAC)

Ivan Saraiva Silva (Federal University of Piauí, Brazil)

XVI Simpósio em Sistemas Computacionais de Alto Desempenho (WSCAD)

Alfredo Goldman (University of São Paulo, Brazil)

Edward David Moreno (Federal University of Sergipe, Brazil)

Luciana Arantes (Pierre et Marie Curie University, France)

Concurso de Teses e Dissertações em Arquitetura de Computadores e Computação de Alto Desempenho (WSCAD-CTD)

Cesar De Rose (Pontifical Catholic University of Rio Grande do Sul, Brazil)

Denise Stringhini (Federal University of São Paulo, Brazil)

Workshop de Iniciação Científica em Arquitetura de Computadores e Computação de Alto Desempenho (WSCAD-WIC)

Carlos Augusto Martins (Pontifical Catholic University of Minas Gerais, Brazil)

Márcia Cristina Cera (Federal University of Pampa, Brazil)

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Events in Portuguese: WSCAD, WEAC, and all meetings.

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Morning

Conference Center 1

11 am – 12:30 pm

WEAC – Sessão 1: Ferramentas de Apoio ao Ensino (Chair: Ivan Silva)

- Ensinando Arquiteturas Vetoriais Utilizando um Simulador de Instruções MIPS. *Fredy Alves, Danilo Almeida, Lucas Bragança, André Gomes, Ricardo Ferreira, José Augusto Nacif*
- IPNoSys IDE - Ambiente de Desenvolvimento e Simulação Integrado para uma Arquitetura não Convencional. *Lucas Oliveira, Silvio Fernandes*
- Uma Análise sobre Ferramentas de Redes-em-Chip e seus Recursos para Uso no Ensino. *Eduardo Silva, Cesar Zeferino*
- Exploring the stack for fun and profit. *Noemi Rodriguez, Ana Lucia de Moura*

Conference Center 2

10 am – 12:30 pm

WAMCA – Session 1: Architecture and Performance Analysis (Chair: Ricardo Farias)

- Using Hardware Transactional Memory to Enable Speculative Trace Optimization. *Juan Salamanca, José Nelson Amaral and Guido Araujo*
- Energy Consumption and Scalability Evaluation for Software Transactional Memory on a Real Computing Environment. *Timoteo Rico, Mauricio Pilla, Andre Rauber Du Bois and Rodrigo Duarte*
- Impact of Version Management on Transactional Memories' Performance. *Felipe Teixeira, Mauricio Pilla, Andre Rauber Du Bois and Daniel Mosse*
- Replicating the Performance Evaluation of a N-Body Application on a Manycore Accelerator. *Vinícius Garcia Pinto, Vinicius Alves Herbstrith and Lucas Schnorr*
- Characterizing Anomalies of a Multicore ARMv7 Cluster with Parallel N-Body Simulations. *Jean Luca Bez, Lucas Mello Schnorr and Philippe Olivier Alexandre Navaux*

- Intra-Clustering: Accelerating On-Chip Communication for Data Parallel Architectures. *Wen Yuan, Rahul Boyapati, Lei Wang, Hyunjun Jang, Ki Hwan Yum and Eun Jung Kim*

Conference Center 3

11 am – 12:30 pm

WSCAD-WIC - Sessão 1: Avaliação, Medição e Predição de Desempenho

- Análise do Desempenho e Consumo de Energia de Aplicações Paralelas com Baixa Demanda de Comunicação. *Thayson Rafael Karlinski, Arthur Lorenzon, Antonio Carlos Beck F., Márcia Cera*
- Estudo Comparativo de Algoritmos para Interseção de Conjuntos Ordenados Utilizando CPU ou GPU. *Italo Milagres, Isaias Frederick, Antonio C. Nazare Jr., Joubert Lima*
- Otimização do Formato Pajé usando Arquivos Binários. *Vinícius Herbstrith, Lucas Schnorr*
- Avaliação de Desempenho de Banco de Dados em Nuvem utilizando o Google Apps Script. *Guilherme Hoffmann, Andrea Charao*
- Exploração de Sequências de Otimizações por Meio de Estimativas de Desempenho. *Vanderson Rosario, Marcos Yukio, Anderson Faustino*
- Proposta de Balanceamento de Carga para Redução de Migração de Processos em Ambientes Multiprogramados. *Guilherme Arruda, Edson Padoin, Laércio Lima Pilla, Philippe Olivier Alexandre Navaux, Jean-François Méhaut*

Afternoon

Ritz Auditorium

3 pm – 4 pm

SBAC-PAD – Session 1: Applications and Algorithms Using Hardware Accelerators

- Towards Seismic Wave Modeling on Heterogeneous Many-core Architectures using Task-based Runtime System. *Victor Martinez, David Michea, Fabrice Dupros, Olivier Aumage, Samuel Thibault, Hideo Aochi and Philippe Navaux*
- Optimized Parallel Label Propagation based Community Detection on the Intel® Xeon Phi™ Architecture. *Andrei Khlopotine*

4:30 pm – 5:30 pm

Sponsor Talk - NEC

Title: NEC SX-ACE Vector Supercomputer and Beyond

5:30 pm – 6:30 pm

Opening Ceremony

Conference Center 1

2 pm – 4 pm

WEAC – Sessão 2: Estudos de Caso (Chair: Silvio Fernandes)

- Aprendendo na Prática: Relato de Sequência de Atividades Práticas em Iniciação Científica Relacionadas à Arquitetura de Computadores. *Francisco Carlos Junior, Tiago Patrocinio, Francisco Alves, Ivan Silva*
- Estudo de Caso sobre o Uso de Realidade Aumentada no Ensino de Arquitetura de Computadores. *Luciano Brum, Leonardo Pinho, Sandro Camargo*
- Proposta de Experimento Didático para Compreensão das Limitações do Uso de Nuvens Computacionais para CAD. *David Willians Beserra, Rubens Paula da Silva, Edward Moreno, Sergio Galdino*
- Análise do Uso de Microcontroladores como Ferramenta de Apoio ao Ensino-Aprendizagem de Arquitetura de Computadores. *Vinícius da Silva, Jean Felipe Patikowski Cheiran*

Conference Center 2

2 pm – 4 pm

WSCAD – Tutorial: Ricardo Farias (UFRJ)

Title: Optimizing Codes on GPUs

Some advances presented in the latest release of Cuda allow further optimizations on some codes. In this tutorial, we will present some its new features and show some case of studies.

Conference Center 3

2 pm – 4 pm

WSCAD-WIC – Sessão 2: Arquitetura de Computadores e Aplicações de Alto Desempenho

- FBT: Um Tradutor Dinâmico de Software para a Arquitetura ARM. *Felipe Carvalho, Edward Moreno*
- Algoritmo de Regras de Associação Paralelo para Arquiteturas Multicore e Manycore. *João de Rezende, Rodrigo Caetano Rocha, Luís Fabrício Wanderley Góes*
- Análises de Sistemas Operacionais Linux usando Plataforma Embarcada. *Victor Gutemberg Santos Lima, Wanderson Roger Azevedo Dias, José Damião de Melo, Edward Moreno*
- Adaptação do Benchmark Lee-TM para Biblioteca de STM TinySTM. *Michael Costa, Felipe Teixeira, Mauricio Pilla, Andre Du Bois*
- Modelagem e Implementação em VHDL de Unidade Aritmética de Ponto Flutuante Segundo o Padrão IEEE-754. *João Pampanini, Cainã Trevisan, Clara Darú, Jean Diogo, Roberto Hexsel*
- StencilBench: Um Benchmark Sintético para Avaliação de Frameworks do Padrão Estêncil. *Alyson Deives Pereira, Sérgio Vitarelli, Rodrigo Caetano Rocha, Márcio Castro, Luís Fabrício Wanderley Góes*
- Modelos de Alocação em Memória da GPU para o Algoritmo de Alinhamento Global de Needleman-Wunsch. *Nilton Queiroz Junior, Ronaldo A. L. Goncalves, Anderson Faustino*
- Avaliação de Desempenho do Método de Lattice Boltzmann em Arquiteturas Multi-core e Many-core. *Matheus Serpa, Claudio Schepke, João Vicente Ferreira Lima*

Conference Center Foyer

4 pm – 4:30 pm

WSCAD-WIC – Sessão de pôsteres

- Abordagem Paralela para o Método de Clustering Search (CS) Aplicado ao Problema de Agrupamento Centrado Capacitado. *Davi Morales, Alvaro Fazenda, Antonio Chaves*
- Aceleração de um Modelo de Simulação de Incêndios em Florestas Usando GPU. *Mauricio Matter Donato, Andrea Charao, Haroldo Campos Velho*
- Adaptação do Algoritmo BMLPA a um Modelo Paralelo Utilizando o Apache Spark. *Marcos Junior, Fábio Zschornack, Mozart Siqueira, Roger Krolow*
- Algoritmos Criptográficos Zorro e AES em FPGAs. *Kaique Menezes, Edward Moreno*
- Analisando o Impacto da Criação Dinâmica de Processos em MPI-2 no Consumo de Memória. *Gabriel Escobar Vasques, Márcia Cera*
- Análise da Escalabilidade de um Algoritmo Genético Paralelizado usando OpenMP. *Mateus Fontoura Gomes da Rosa, Márcia Cera*
- Comparação de Rastros de Execução Utilizando um Algoritmo de Alinhamento de Sequências. *Alef Farah, Lucas Schnorr*
- Gerenciamento do Motor Gerador de Containers para Nuvens Computacionais. *Allan Santos, Henrique Klôh, Jonathan Barbosa, Bruno Schulze*
- Implantação e Avaliação de Desempenho de um Cluster Raspberry Pi com NAS Parallel Benchmarks. *Gabriel Garcia, Henrique C. Freitas*
- qExVHDL: Extensão do Simulador Quântico em VHDL. *Lucas Agostini, Julio Neto, Cristian Bosin, Bruno Zatt, Mauricio Pilla, Renata Reiser*
- Uma Abordagem para o Escalonamento Virtual Utilizando Computação Paralela Distribuída para o Processamento de Jogos MMOGS. *Eduardo Tosin, Wander Scheid, Mario Dantas*

Monday, October 19

Events in English: SBAC-PAD, Keynotes, Sponsor Talks, WAMCA, MPP, and the Parallel Programming Marathon.
Events in Portuguese: WSCAD, WEAC, and all meetings.

Time GMT-2	Monday, October 19			
	Ritz Auditorium	CC1	CC2	CC3
8:00 8:30	Registration Desk			
9:00 9:30	Keynote Geoffrey Fox			
10:00	Coffee-Break + WSCAD-WIC Posters Ritz Auditorium Foyer			
10:30 11:00	SBAC-PAD 2 - ACC	WSCAD-CTD M.Sc.	Maratho Warmup	WSCAD 1 - ACC
11:30 12:00	Sponsor Talk Cray			
12:30 13:00 13:30	Lunch (included for all participants) Exposition Center - Majestic Palace Hotel			
14:00 14:30 15:00 15:30	SBAC-PAD 3 - Arch.	WAMCA 2 - AAPM	Marathon	WSCAD 2 - Embed. & Energy
16:00	Coffee-Break Conference Center Foyer			
16:30 17:00	Sponsor Talk Bull		Marathon	
17:30 18:00 18:30	SBAC-PAD 4 - Mem.	WAMCA 3 - FBT		CRADs Meeting
19:00 19:30 20:00				CEACPAD Meeting

Morning

Ritz Auditorium

9 am – 10 am

SBAC-PAD – Keynote 1: Geoffrey Charles Fox (Indiana University, USA)

Talk: Big Data Applications, Software and System Architectures

We discuss the nexus of big data applications, software and infrastructure where we identify 6 overall machine architectures. The big data applications are drawn from a study from NIST and the layered software from a compendium of open-source, commercial and HPC systems. We illustrate with typical "big data analytics" machine learning with varied Parallel Programming Models (MPI, Hadoop, Spark, Storm) on both cloud and HPC platforms. We discuss performance (of Java) and the use of DevOps scripts such as Chef/Ansible and OpenStack Heat to specify software stack. This leads to the interesting virtual cluster concept.

10:30 am – 11:30 am

SBAC-PAD – Session 2: Applications and Algorithms Using Hardware Accelerators

- GPU-accelerated High-speed Eye Pupil Tracking System. *Juan Mompeán, Juan L. Aragón, Pablo Artal and Pedro Prieto*
- Efficient Irregular Wavefront Propagation Algorithms on Intel Xeon Phi. *Jeremias Moreira, George Teodoro, Alba Melo, Jun Kong, Tahsin Kurc and Joel Saltz*

11:30 am – 12:30 pm

Sponsor Talk - Cray

Title: Adaptive Supercomputing

Conference Center 1

10:30 am – 11:30 am

WSCAD-CTD - Sessão 1: Melhores Dissertações de Mestrado

- Soluções em GPU para o Problema do Alinhamento Spliced. *Anisio Nolasco, Nahri Moreano*
- Eliot - Uma Arquitetura para Internet das Coisas: Explorando a Elasticidade da Computação em Nuvem com Alto Desempenho. *Marcio Gomes, Cristiano Costa, Rodrigo Righi*
- Integração de Características Preemptivas à Técnica de Escalonamento Dinâmico de Tensões e Frequências Intra-Tarefa. *Rawlinson Gonçalves, Raimundo Barreto*

Conference Center 2

10:30 am – 12:30 pm

Parallel Programming Marathon – Warmup

Conference Center 3

10:30 am – 11:30 am

WSCAD – Sessão 1: CUDA - GPU and SIMD Vector (Chair: Alba Melo)

- Accelerating Pre-stack Kirchhoff Time Migration by using SIMD Vector Instructions. *Maicon Alves, Lucia Drummond, Reynam Pestana*
- Autotuning GPU Compiler Parameters Using OpenTuner. *Pedro Bruel, Alfredo Goldman, Marcos Amaris*
- Verificação de Kernels em Programas CUDA Usando Bounded Model Checking. *Phillipe Pereira, Higo Albuquerque, Hendrio Marques, Isabela Silva, Vanessa Santos, Ricardo Ferreira, Celso Carvalho, Lucas Cordeiro*

Ritz Auditorium Foyer

10 am – 10:30 am

WSCAD-WIC – Sessão de pôsteres

Afternoon

Ritz Auditorium

2 pm – 4 pm

SBAC-PAD – Session 3: New Architectures and Hardware Mechanisms to Improve Performance

- Performance and Energy Efficient Hardware-based Scheduler for Symmetric/Asymmetric CMPs. *Nikola Markovic, Daniel Nemirovsky, Osman Unsal, Mateo Valero and Adrian Cristal*
- Analysis and Optimization of Engines for Dynamically Typed Languages. *Gem Dot, Alejandro Martínez and Antonio González*
- Memory Centric Computation (mc2) for Large-scale Graph Processing. *Kattamuri Ekanadham and Guojing Cong*
- Progressive Codesign of an Architecture and Compiler using a Proxy Application. *Arpith Jacob, Tong Chen, Zehra Sura, Changhoan Kim, Carlo Bertolli, Samuel Antao, Kevin O'Brien and Ravi Nair*

4:30 pm – 5:30 pm

Sponsor Talk - Bull

Title: From Petascale to Exascale - A Pragmatic Approach

5:30 pm – 7 pm

SBAC-PAD – Session 4: Memory Systems and Optimizations

- Tidy Cache: Improving Data Placement in Die-stacked DRAM Caches. *Adrià Armejach, Adrian Cristal and Osman S. Unsal*
- Unifying Router Power Gating with Data Placement for Energy-Efficient NoC. *Yuho Jin*
- i-MIRROR: A Software Managed Die-Stacked DRAM-Based Memory Subsystem. *Jee Ho Ryoo, Karthik Ganesan, Yao-Min Chen and Lizy John*

Conference Center 1

2 pm – 4 pm

WAMCA – Session 2: Applications, Algorithms and Programming Models (Chair: Maurício Pilla)

- Many SVDs on GPU for Image Mosaic Assemble. *Irving S. Badolato, Luciano L. V. de Paula and Ricardo Farias*
- MDACCER: Modified Distributed Assessment of the Closeness CEntrality Ranking in Complex Networks for Massively Parallel Environments. *Frederico Cabral, Carla Osthoff Barros, Daniel Nascimento and Rafael Nardes*
- A Performance Study on GPU-based Neighborhood Search Algorithms for Vehicle Routing. *Eyder Rios, Luiz Satoru Ochi, Cristina Boeres, Igor M. Coelho and Ricardo Farias*
- Evaluating Overhead and Contention in Concurrent Accesses to a Graph. *Israel Barbará, Nicolas de Araújo, André Du Bois and Gerson Cavalheiro*
- Single-Loop Approach to 2-D Wavelet Lifting with JPEG 2000 Compatibility. *David Barina, Petr Musil, Martin Musil and Pavel Zemcik*
- On the Evaluation of Contention-Aware List Schedulers on Multicore Cluster. *Juliana Zamith, Thiago Silva, Lucia Drummond, Cristina Boeres and Cristiana Bentes*

5:30 pm – 7 pm

WAMCA – Session 3: Frameworks, Benchmarking and Tools (Chair: Ricardo Farias)

- Kanga: a Skeleton-Based Generic Interface for Parallel Programming. *Bruno Pinto, Daves Kist, André Du Bois and Gerson Cavalheiro*
- Painless Parallelism on Heterogeneous Hardware Leveraging the Functional Paradigm. *Mauro Blanco, Pablo Perdomo, Pablo Ezzatti, Alberto Pardo and Marcos Viera*
- CoBaS: Introducing a Component Based Scheduling Framework. *Anselm Busse, Reinhardt Karnapke and Hans-Ulrich Heiss*
- CHAOS-MCAPI: An Optimized Mechanism to Support Multicore Parallel Programming. *Antonio Diogo Hidee Ideguchi, Célio Estevam Morón and Marcio Merino Fernandes*

Conference Center 2

2 pm – 7 pm

Parallel Programming Marathon

Conference Center 3

2 pm – 4 pm

WSCAD – Sessão 2: Embedded Architectures and Energy Consumption (Chair: Leandro Marzulo)

- Relógio Virtual Estritamente Crescente para o Computador Raspberry PI. *Edilson Corrêa, Diego Dutra, Claudio Amorim*
- COISA: A Compact OpenISA virtual platform for IoT devices. *Carlos Millani, Alisson Linhares, Rafael Auler, Edson Borin*
- Exploração de Desempenho, Consumo Dinâmico e Eficiência Energética em MPSoCs. *Liana Duenha, Rodolfo Azevedo, Fernando Moraes, Guilherme Madalozzo, Thiago Santiago*
- Avaliação de um Framework de Apoio ao Desenvolvimento de Heurísticas de Escalonamento Sensível ao Consumo Energético. *Bruno Pinto, Lucas Xavier, Gerson Geraldo H. Cavalheiro*

5:30 pm – 6:30 pm

CRADs – Meeting

6:30 pm – 8:30 pm

CEACPAD – Meeting

Tuesday, October 20

Events in English: SBAC-PAD, Keynotes, Sponsor Talks, WAMCA, MPP, and the Parallel Programming Marathon.
Events in Portuguese: WSCAD, WEAC, and all meetings.

Time GMT-2	Tuesday, October 20			
	Ritz Auditorium	**CC1**	**CC2**	**CC3**
8:00 8:30	Registration Desk			
9:00 9:30	Keynote Satoshi Matsuoka			
10:00	Coffee-Break Ritz Auditorium Foyer			
10:30 11:00	SBAC-PAD 5 - Code Opt.	WSCAD-CTD Ph.D.	Sponsor Talk SGI	WSCAD 3 - Multicore
11:30 12:00	Sponsor Talk Supermicro			
12:30 13:00 13:30	Lunch (included for all participants) Exposition Center - Majestic Palace Hotel			
14:00 14:30 15:00 15:30	SBAC-PAD 6 - Eval.	MPP Invited Talk MPP 1	SBAC-PAD Tutorial 1	WSCAD 4 - Sched.
16:00	Coffee-Break Conference Center Foyer			
16:30 17:00	Sponsor Talk Intel			
17:30 18:00 18:30	SBAC-PAD 7 - FT & Storage	MPP 2	CRAD-SP Meeting	WSCAD 5 - Algorithms
19:00 19:30				
20:00	Conference Dinner & Awards Ceremony Maria do Mar Hotel			

Morning

Ritz Auditorium

9 am – 10 am

SBAC-PAD – Keynote 2: Satoshi Matsuoka (Global Scientific Information and Computing Center, Tokyo Institute of Technology, Japan)

Talk: The Inevitable End of Moore's Law Beyond Exascale Will Cause Big Data and HPC Convergence

The so-called "Moore's Law", by which the performance of the processors will increase exponentially by factor of 4 every 3 years or so, is slated to be ending in 10-15 year timeframe due to the lithography of VLSIs reaching its limits around that time, and combined with other physical factors. This is largely due to the transistor power becoming largely constant, and as a result, means to sustain continuous performance increase must be sought otherwise than increasing the clock rate or the number of floating point units in the chips, i.e., increase in the FLOPS. The promising new parameter in place of the transistor count is the perceived increase in the capacity and bandwidth of storage, driven by device, architectural, as well as packaging innovations: DRAM-alternative Non-Volatile Memory (NVM) devices, 3-D memory and logic stacking evolving from VIAs to direct silicone stacking, as well as next-generation terabit optics and networks. The overall effect of this is that, the trend to increase the computational intensity as advocated today will no longer result in performance increase, but rather, exploiting the memory and bandwidth capacities will instead be the right methodology. However, such shift in compute-vs-data tradeoffs would not exactly be return to the old vector days, since other physical factors such as latency will not change. As such, performance modeling to account for the evolution of such fundamental architectural change in the post-Moore era would become important, as it could lead to disruptive alterations on how the computing system, both hardware and software, would be evolving towards the future.

10:30 am – 11:30 am

SBAC-PAD – Session 5: Code Optimization

- Fusion of Calling Sites. *Douglas Teixeira, Sylvain Collange and Fernando Pereira*
- OpenCL Kernel Fusion for GPU, Xeon Phi and CPU. *Jiří Filipovič and Siegfried Benkner*

11:30 am – 12:30 pm

Sponsor Talk - Supermicro

Title: The New Era of Coprocessor for Parallel Processing: Designing Coprocessor Optimized HPC Solutions

Conference Center 1

10:30 am – 11:30 am

WSCAD-CTD - Sessão 2: Melhores Teses de Doutorado

- Transversal I/O scheduling for Parallel File Systems: From Applications to Devices. *Francieli Boito, Philippe Olivier Alexandre Navaux, Yves Denneulin*
- Application-Aware Software-Defined Networking to Accelerate MapReduce Applications. *Marcelo Neves, Cesar De Rose*
- Avaliação de Sistemas de Computação Massivamente Paralela e Distribuída: Uma Metodologia Voltada aos Requisitos das Aplicações Científicas. *Mariza Ferro, Bruno Schulze*

Conference Center 2

10:30 am – 11:30 am

Sponsor Talk - SGI

Title: Dawn of a New HPC Centre: Facts, Figures & Case Studies

Conference Center 3

10:30 am – 11:30 am

WSCAD – Sessão 3: Multicore and Many-core Architectures (Chair: Ivan Silva)

- How Run Your Simulation in Many-cores without Change Neither the SystemC nor Yours Modules. *Tiago Falcão, Liana Duenha, Rodolfo Azevedo*
- Identificação Automática de Dark Silicon em Processadores Multicore. *Ana Silva, Tony Bignardi, Edilson Palma, Rafael da Costa, Clara Silva, Ricardo Santos*
- Portabilidade com Eficiência da Advecção do Modelo BRAMS entre Arquiteturas Multi-Core e Many-Core. *Manoel Júnior, Jairo Panetta, Stephan Stephany*

Afternoon

Ritz Auditorium

2 pm – 4 pm

SBAC-PAD – Session 6: System Characterization and Performance Evaluation

- WattWatcher: Fine-Grained Power Estimation For Emerging Workloads. *Michael Lebeane, Jee Ho Ryoo, Reena Panda and Lizy John*
- Performance Characterization of Modern Databases on Out-of-order CPUs. *Reena Panda, Christopher Erb, Michael Lebeane, Jeeho Ryoo and Lizy Kurian John*
- Cloud Services Evaluation through QoE: A Methodological Approach. *Frederico Guilherme Irigoyen Da Costa, Maria Cristina Felippetto de Castro, Candice Muller and Fernando C. C. De Castro*
- Non-stationary Simulation of Computer Systems and Dynamic Performance Evaluation: a Concern-based Approach and Case Study on Cloud Computing. *Lourenço Alves Pereira Júnior, Edwin Luis Choquehuanca Mamani, Marcos José Santana, Regina Helena Carlucci Santana, Pedro Northon Nobile and Francisco José Monaco*
- Serialization Management for Best-Effort Hardware Transactional Memory: A key for performance. *Matthew Gaudet, Jose Nelson Amaral and Guido Araujo*

4:30 pm – 5:30 pm

Sponsor Talk - Intel

Title: Driving Faster Breakthroughs Through Code Modernization for Today's and Tomorrow's Hardware on Intel® Architecture

5:30 pm – 7 pm

SBAC-PAD – Session 7: Fault Tolerance and Cloud Storage

- Exploring Energy-Consistency Trade-off in Cassandra Cloud Storage System. *Houssem-Eddine Chihoub, Shadi Ibrahim, Yue Li, Gabriel Antoniu, Maria S. Perez and Luc Bougé*
- COMET: Client-Oriented Metadata Service for Highly Available Distributed File Systems. *Ruini Xue, Lixiang Ao and Zhongyang Guan*

- A Fault-Tolerance Protocol for Parallel Applications with Communication Imbalance. *Esteban Meneses and Laxmikant Kale*

Conference Center 1

2 pm – 3 pm

MPP – Invited Speaker: Andrew Putnam (Microsoft, USA)

3 pm – 4 pm

MPP – Session 1

- Graph Templates for Dataflow Programming. *Leandro A. J. Marzulo, Tiago Alves, Alexandre Sena, Felipe M. G. França and Eduardo Vaz*
- A Parallel Implementation of Data Fusion Algorithm Using Gamma. *Rui Rodrigues de Mello Junior, Gabriel Antoine Louis Paillard, Rubens Henrique Pailo de Almeida and Felipe Maia Galvão França*

5:30 pm – 7 pm

MPP – Session 2

- Exploiting Parallelism in Linear Algebra Kernels through Dataflow Execution. *Brunno Goldstein, Leandro A. J. Marzulo, Tiago Alves and Felipe M. G. França*
- A Parallel Algorithm for the Facility Location Problem Applied to Oil and Gas Logistics. *Thiago Pinheiro and Maria Clicia Castro*
- RadFlow: An Interest-centric Task-based Dataflow Runtime. *Diego Dutra, Héberte Moraes and Claudio Amorim*

Conference Center 2

2 pm – 4 pm

SBAC-PAD – Tutorial 1: Luiz DeRose (Cray Inc.)

Title: Challenges in Creating Performance Portable Applications for the New Generation of Supercomputers

Are you ready for the future of high performance computing? Is your application performance portable? The scale and complexity of high-end systems is increasing, nodes are becoming more parallel with many processors per node, more threads per processor, longer vector lengths, more complex memory hierarchies, and potentially heterogeneous processing elements. These technology changes in the supercomputing industry are forcing computational scientists to address new critical system characteristics that will significantly impact the performance and scalability of applications. These considerations will require a

paradigm shift in application development. One main change is that the dominant programming model of parallelism through only message passing will not be feasible on this new generation of high performance systems. Application developers will have to hybridize their codes, adding multiple levels of parallelism. In addition, since these systems may have heterogeneous processors and multiple levels of the memory hierarchy, application developers may also have to introduce pragmas or directives for better node utilization and performance portability across a wide range of systems. In this tutorial I will discuss these trends in the supercomputing industry, including programming paradigms and tools to support porting and tuning efforts, and will also discuss some of the challenges and open research problems that need to be addressed to create applications and build system software for the new generation of high performance computing systems.

5:30 pm – 7:30 pm

CRAD-SP – Meeting

Conference Center 3

2 pm – 4 pm

WSCAD – Sessão 4: Scheduling and Applications (Chair: Eduardo Rocha Rodrigues)

- Impacto de Estratégias Combinatórias no Precondicionador Paralelo Híbrido SPIKE. *Brenno Lugon, Lucia Catabriga, Maria Cristina Rangel, Leonardo Lima*
- Improving the Performance of the Contextual Spaces Re-Ranking Algorithm on Heterogeneous Systems. *Flávia Pisani, Daniel Pedronette, Ricardo Torres, Edson Borin*
- Scheduling Moldable BSP Tasks on Clouds. *Thiago Okada, Marcos Amaris, Alfredo Goldman*
- Uma Metodologia Baseada em Simulação e Algoritmo Genético para Projeto e Exploração de Estratégias de Escalonamento de Laços. *Pedro Henrique Penna, Márcio Castro, Henrique C. Freitas, François Broquedis, Jean-François Méhaut*
- The Case for Resource Sharing in Scientific Workflow Executions. *Ricardo Oda, Daniel Cordeiro, Kelly Braghetto, Rafael Ferreira da Silva, Ewa Deelman*

5:30 pm – 7 pm

WSCAD – Sessão 5: Algorithms and Applications (Chair: Lucia Catabriga)

- Comparando o Desempenho de Implementações de Tabelas Hash Concorrentes em Haskell. *Rodrigo Duarte, Andre Du Bois, Mauricio Pilla, Renata Reiser*
- Construção Paralela de Árvores de Cortes Utilizando Contrações de Grafo Otimizadas. *Jaime Cohen, Elias Duarte Jr., Charles Maske*
- Otimização de Simulação de Computação Quântica Através da Redução e Decomposição Baseados no Operador Identidade. *Anderson Avila, Renata Reiser, Mauricio Pilla*
- Reavaliando o Conjunto de Aplicações STAMP em um Novo Hardware Transacional. *João Paulo de Carvalho, Alexandro Baldassin, Rafael Murari*

Wednesday, October 21

Events in English: SBAC-PAD, Keynotes, Sponsor Talks, WAMCA, MPP, and the Parallel Programming Marathon.
Events in Portuguese: WSCAD, WEAC, and all meetings.

Time GMT-2	Wednesday, October 21			
	Ritz Auditorium	CC1	CC2	CC3
8:00	Registration Desk			
8:30				
8:45	Keynote Onur Mutlu			
9:30				
10:00	Coffee-Break Ritz Auditorium Foyer			
10:30	SBAC-PAD 8 - Sched. & VM	WEAC Meeting		WSCAD 6 - Low Cost HPC
11:00				
11:30	Sponsor Talk HP			
12:00				
12:30	Lunch			
13:00				
13:30				
14:00	SBAC-PAD 9 - Sched. & VM		SBAC-PAD Tutorial 2	
14:30				
15:00				
15:30				

Morning

Ritz Auditorium

8:45 am – 10 am

SBAC-PAD – Keynote 3: Onur Mutlu (Carnegie Mellon University, USA)

Title: Rethinking Memory System Design for Data-Intensive Computing

The memory system is a fundamental performance and energy bottleneck in almost all computing systems. Recent system design, application, and technology trends that require more capacity, bandwidth, efficiency, and predictability out of the memory system make it an even more important system bottleneck. At the same time, DRAM and flash technologies are experiencing difficult technology scaling challenges that make the maintenance and enhancement of their capacity, energy-efficiency, and reliability significantly more costly with conventional techniques.

In this talk, we examine some promising research and design directions to overcome challenges posed by memory scaling. Specifically, we discuss three key solution directions: 1) enabling new memory architectures, functions, interfaces, and better integration of the memory and the rest of the system, 2) designing a memory system that intelligently employs multiple memory technologies and coordinates memory and storage management using non-volatile memory technologies, 3) providing predictable performance and QoS to applications sharing the memory/storage system. If time permits, we might also briefly touch upon our ongoing related work in combating scaling challenges of NAND flash memory.

10:30 am – 11:30 am

SBAC-PAD – Session 8: Scheduling and Virtual Machines

- Comparison of Static and Runtime Resource Allocation Strategies for Matrix Multiplication. *Olivier Beaumont, Lionel Eyraud-Dubois, Abdou Guermouche and Thomas Lambert*
- Device-Sensitive Framework for Handling Heterogeneous Asymmetric Clusters Efficiently. *Valon Raca and Eduard Mehofer*

11:30 am – 12:30 pm

Sponsor Talk - HP

Title: The HP HPC Solutions

Conference Center 1

10:30 am – 11:30 am

WEAC – Meeting (Chair: Carlos Augusto P. da S. Martins)

Conference Center 3

10:30 am – 11:30 am

WSCAD – Sessão 6: Low Cost Platforms and HPC (Chair: Maurício Pilla)

- Análise da Eficiência Energética de uma Aplicação HPC de Geofísica em um Cluster de Baixo Consumo. *Jean Luca Bez, Eliezer Bernart, Fernando dos Santos, Lucas Schnorr, Philippe Olivier Alexandre Navaux*
- Avaliação do Consumo de Energia na Execução do NAS Parallel Benchmark (NPB) em Processadores ARM. *Alexandre Carissimi, Jorge Ximendes da Silva Junior*
- Utilização de Aceleradores Embarcados de Baixo Consumo na Implementação de Sistemas de HPC. *Edson Padoin, Emilio Hoffmann, Jorge Silva Jr., Philippe Olivier Alexandre Navaux*

Afternoon

Ritz Auditorium

2 pm – 3:30 pm

SBAC-PAD – Session 9: Scheduling and Virtual Machines

- Evaluating the Impact of Memory Allocation and Swap for Vertical Memory Elasticity in VMs. *Roberto Sawamura, Cristina Boeres and Vinod Rebello*
- Quantum Virtual Machine: a Scalable Model to Optimize Energy Savings and Resource Management. *Andre Felipe Monteiro and Orlando Loques*
- A Programming Interface for Overload Control in Staged Event-based Architectures. *Breno Cruz, Noemi Rodriguez and Ana Lúcia Moura*

Conference Center 2

2 pm – 4 pm

SBAC-PAD – Tutorial 2: Esteban Meneses (Costa Rica Institute of Technology, Costa Rica), Celso. L. Mendes (National Center for Supercomputing Applications, USA) and Laércio L. Pilla (Federal University of Santa Catarina, Brazil)

Title: Programming with Parallel Objects: from MPI to Charm++

Programming large supercomputers presents several challenges: exposing concurrency, controlling load imbalance, tolerating failures, among others. Addressing these challenges requires an emphasis on important concepts during application development: overdecomposition, asynchrony, migratability, and adaptivity. This tutorial presents Charm++, a programming paradigm that encapsulates these ideas. Charm++ provides an asynchronous, message-driven programming model via parallel objects and an adaptive runtime system that guides execution. It automatically overlaps communication and computation, balances loads, tolerates failures, checkpoints for split-execution, and promotes modularity while allowing programming in C++. Several widely used Charm++ applications thrive in computational science domains including biomolecular modeling and cosmology. The approach followed in this tutorial provides a guide for migrating applications from the reigning parallel programming paradigm (MPI) to Charm++.